

## Claims

What is claimed is:

- 5 1. A method for providing simultaneous bidirectional signaling in a bus topology comprising the steps of:
- 10 selecting a first device and a second device from among a plurality of devices operably coupled to a common bus to exchange a first set of data;
- scheduling a first exchange slot over which the first device and the second device are to exchange the first set of data; and
- 15 during the first exchange slot, simultaneously transmitting a first portion of the first set of data from the first device to the second device over the common bus and transmitting a second portion of the first set of the data from the second device to the first device over the common bus.
2. The method of claim 1 further comprising the steps of:
- selecting the first device and a third device to exchange a second set of data;
- scheduling a second exchange slot over which the first device and the third device are to exchange the second set of data; and
- 20 during the second exchange slot, simultaneously transmitting a first portion of the second set of data from the first device to the third device over the common bus and transmitting a second portion of the second set of the data from the third device to the first device over the common bus.
- 25 3. The method of claim 2 further comprising the step of:
- introducing a turnaround delay between the first exchange slot and the second exchange slot.
4. The method of claim 3 wherein the turnaround delay is less than twice an end-to-
- 30 end propagation delay of the common bus.

5. The method of claim 1 wherein the first device is a memory controller, and the second device is a memory device and wherein the first portion of the first set of data and the first portion of the second set of data are write data and the second portion of the first set of data and the second portion of the second set of data are read data.

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6. A system providing simultaneous bidirectional signaling using a bus topology, the system comprising:

a first device operably coupled to a bus;

5 a second device operably coupled to the bus, the first device transmitting a first portion of a first set of data to the second device and the second device transmitting a second portion of the first set of data to the first device simultaneously during a first exchange slot; and

10 a third device operably coupled to the bus, the first device transmitting a first portion of a second set of data to the third device and the third device transmitting a second portion of the second set of data to the first device simultaneously during a second exchange slot.

7. The system of claim 6 wherein a turnaround delay exists between the first exchange slot and the second exchange slot.

15 8. The system of claim 7 wherein the turnaround delay is less than twice an end-to-end propagation delay of the bus.

20 9. The system of claim 6 wherein the first device is a memory controller, and the second device is a memory device and wherein the first portion of the first set of data and the first portion of the second set of data are write data and the second portion of the first set of data and the second portion of the second set of data are read data.

10. A device coupled to a bus in a bus topology capable of simultaneous bidirectional signaling, the device comprising:

a driver capable of additive signaling, said driver circuit applying transmit signals to the bus;

5 a receiver circuit operably coupled to the driver, the receiver circuit capable of effectively subtracting the transmit signals to receive received signals from the bus, the driver and the receiver circuit operating during an exchange slot.

11. The device of claim 10 wherein the device is coupled to the bus by an impedance-  
10 matching splitter.

12. The device of claim 10 wherein the device further comprises:

a terminator operably coupled to the driver and the receiver circuit, the terminator providing a controlled termination impedance.

13. The device of claim 10 wherein the device further comprises:

a transmit circuit operably coupled to the driver, the transmit circuit comprising a transmit buffer, the transmit buffer holding data pending arrival of the exchange slot.

14. The device of claim 13 wherein the transmit buffer further comprises:

a plurality of transmit buffers, the plurality of transmit buffers adaptable to hold data destined for different other devices.

15. The device of claim 13 wherein the receiver circuit further comprises:

25 a comparator operably coupled to the transmitter and to the driver, the comparator adaptable to effectively subtract the transmit signals to yield received signals from the bus; and

a receiver operably coupled to the comparator, the receiver receiving the received signals and obtaining received data from the received signals.

16. The device of claim 15 further comprising:  
a circuit responsive to an exchange slot indication, the circuit enabling the operation of the transmit circuit and the receive circuit during the exchange slot.

17. A memory system comprising:

a memory controller;

a bus operably coupled to the memory controller;

a first memory device operably coupled to the bus, the first memory device

5 adapted to simultaneously send first read data to the memory controller via the bus and receive first write data from the memory controller via the bus; and

a second memory device operably coupled to the memory controller, the second memory device adapted to simultaneously send second read data to the memory controller via the bus and receive second write data from the memory controller via the  
10 bus.

18. The memory system of claim 17 wherein the first memory device is adapted to simultaneously send the first read data to the memory controller and receive the first write data from the memory controller during a first exchange slot and wherein the

15 second memory device is adapted to simultaneously send the second read data to the memory controller and receive the second write data from the memory controller during a second exchange slot.

19. The memory system of claim 18 wherein the memory controller comprises:

20 a first write buffer to hold the first write data pending arrival of the first exchange slot.

20. The memory system of claim 19 wherein the memory controller comprises:

25 a second write buffer to hold the second write data pending arrival of the second exchange slot.

21. The memory system of claim 17 wherein the bus comprises:

a conductor operably coupling the first memory device and the second memory device to the memory controller, wherein the first memory device is adapted to  
30 simultaneously send a first read bit of the first read data to the memory controller over the conductor and receive a first write bit of the first write data from the memory controller

over the conductor during a first exchange slot and wherein the second memory device is adapted to simultaneously send a second read bit of the second read data to the memory controller over the conductor and receive a second write bit of the second write data from the memory controller over the conductor during a second exchange slot.

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22. The memory system of claim 21 wherein a turnaround delay sufficient to prevent inter-symbol interference is introduced between the first exchange slot and the second exchange slot.

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23. The memory system of claim 17 wherein the memory controller performs coherency checking during memory access operations.

24. A memory device adaptable to be coupled to a bus comprising:  
a driver adapted to drive the bus with read data during an exchange slot while  
write data are present on the bus;  
a receiver circuit operably coupled to the driver, the receiver circuit capable of  
5 receiving the write data from the bus during the exchange slot while the driver is driving  
the bus with the read data; and  
a memory circuit operably coupled to the receiver circuit, the memory circuit  
adapted to provide the read data and to store the write data.

10 25. The memory device of claim 24 further comprising:  
a circuit responsive to an exchange slot indication, the circuit operably coupled to  
the driver and the receiver circuit, the circuit enabling interaction of the driver and the  
receiver circuit with the bus during the exchange slot.

15 26. The memory device of claim 25 wherein the circuit is adapted to be responsive to  
the exchange slot indication following a turnaround delay sufficient to prevent inter-  
symbol interference.

20 27. The memory device of claim 24 further comprising:  
a transmit circuit operably coupled to the driver, the transmit circuit comprising a  
transmit buffer, the transmit buffer holding the read data pending arrival of the exchange  
slot.



28. A memory controller adapted to be coupled to a bus comprising:  
a driver adapted to drive the bus with first write data destined for a first memory device during a first exchange slot while first read data from the first memory device are present on the bus;

5 a receiver circuit operably coupled to the driver, the receiver circuit adapted to receive the first read data from the bus during the first exchange slot while the driver is driving the bus with the first write data.

29. The memory controller of claim 28 wherein the driver is further adapted to drive  
10 the bus with second write data destined for a second memory device during a second exchange slot while second read data from the second memory device are present on the bus and wherein the receiver circuit is further adapted to receive the second read data from the bus during the second exchange slot while the driver is driving the bus with the second write data.

15 30. The memory controller of claim 29 wherein a turnaround delay sufficient to prevent inter-symbol interference is introduced between the first exchange slot and the second exchange slot.

20 31. The memory controller of claim 28 further comprising:  
a transmit circuit operably coupled to the driver to transmit the first write data and the second write data to the driver, the transmit circuit comprising a transmit buffer to hold the first write data pending arrival of the first exchange slot and the second write data pending arrival of the second exchange slot.

25 32. The memory controller of claim 31 wherein the transmit buffer comprises:  
a first transmit buffer to hold the first write data pending arrival of the first exchange slot; and

30 a second memory buffer to hold the second write data pending arrival of the second exchange slot.

33. A method for providing simultaneous bidirectional communication between a memory controller and a plurality of memory devices comprising the steps of:

during a first exchange slot, simultaneously communicating over a common bus first write data from the memory controller to a first memory device of the plurality of memory devices and first read data from the first memory device to the memory controller; and

during a second exchange slot, simultaneously communicating over a common bus second write data from the memory controller to a second memory device of the plurality of memory devices and second read data from the second memory device to the memory controller.

34. The method of claim 33 further comprising the step of:

holding the first write data destined for the first memory device in the memory controller pending arrival of the first exchange slot.

35. The method of claim 34 further comprising the step of:

holding the second write data destined for the second memory device in the memory controller pending arrival of the second exchange slot.

36. The method of claim 35 wherein the step of holding the first write data occurs in a first write buffer and wherein the step of holding the second write data occurs in a second write buffer.

37. The method of claim 35 further comprising the steps of:

holding the first read data destined for the memory controller in the first memory device; and

holding the second read data destined for the memory controller in the second memory device.

38. The method of claim 37 wherein the step of simultaneously communicating over the common bus the first write data from the memory controller to the first memory

device and the first read data from the first memory device to the memory controller occurs after a specified amount of the first write data destined for the first memory device is held in the memory controller.

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39. A system for bidirectional communication of data over a common bus comprising:

a first device operably coupled to the common bus, the first device comprising a first-to-second transmit buffer to hold first-to-second data and a first-to-third transmit  
5 buffer to hold first-to-third data;

a second device operably coupled to the common bus, the second device comprising a second-to-first transmit buffer to hold second-to-first data;

a third device operably coupled to the common bus, the third device comprising a third-to-first transmit buffer to hold third-to-first data;

10 a scheduler operably coupled to the common bus, the scheduler scheduling the first device to transmit the first-to-second data and the second device to transmit the second-to-first data over the common bus during a first exchange slot and scheduling the first device to transmit the first-to-third data and the third device to transmit the third-to-  
15 a turnaround delay sufficient to prevent inter-symbol interference between the first exchange slot and the second exchange slot.